10. (Amended) The method according to claim 7, wherein the depositing of the fourth insulating film includes depositing by a chemical vapor deposition method or a sputtering method.

A6 (concluded)

12. (Amended) The method according to claim 7, wherein the depositing of the fourth insulating film includes using an insulating material having a dielectric constant of above 5.

13. (Amended) The method according to claim 7, wherein the depositing of the fourth insulating film includes using an insulating material selected from the group consisting of Ta2O5, silicon nitride, Al2O3, BaSrTiO3, Zr oxide, Hf oxide, Sc oxide, Y oxide and Ti oxide.

B1 cont

REMARKS

Favorable reconsideration of this application in view of the following remarks is respectfully requested.

Claims 1-3, 5-10 and 12-18 are presented for examination on this application. Claims 4 and 11 have been canceled without prejudice or disclaimer, Claims 14-18 have been withdrawn from consideration, and Claims 1-3, 5-10, 12, and 13 have been amended without the introduction of any new matter to better highlight the present invention.

The outstanding Office Action included an objection to the title, an objection to the use of "etc." in the specification, an objection to Figs. 1-8, and a rejection of Claims 1-13 under 35 U.S.C. § 103(a) over what is alleged in the outstanding Action to be "Applicant's Admitted Prior Art" (AAPA) in view of Yu (U.S. Patent No. 6,225,173).

With regard to the objection to the Title, it is believed that the present amendment overcomes this objection by presenting the presently amended new title that is believed to be

clearly indicative of the invention to which the claims are directed. Accordingly, withdrawn of this objection is believed to be in order.

With further regard to the objection to the use of "etc." in the specification, the various occurrences of the use of the objected to term have been corrected to recite --for example--. Accordingly, withdrawal of this objection is also believed to be in order.

Turning to the objection raised as to Figures 1-8, an appropriate legend --BACKGROUND ART-- has been added in the attached drawing correction letter submitted for Examiner approval. Accordingly, it is believed that this objection has also been answered and should be withdrawn as well.

Before considering the obviousness rejection, it is believed that a brief review of the present invention would be helpful. In this respect, the invention relates to a method of making an insulated gate field effect transistor that uses a buried type gate electrode structure that avoids gate offset. In accordance with this method, a buried type gate electrode structure is formed using a dummy electrode as shown, for example, relative to Figure 12. The gate length of this dummy electrode is coincident with the final gate length as noted in the specification at page 12, lines 11-12, for example. After the trench is formed by removing the dummy electrode, this trench is broadened on both sides thereof by a predetermined width amount which is equal to or slightly greater than the thickness of the gate insulating film to be formed later. Note, for example, page 14, lines 9-15. As shown in Figures 15 and 16, for example, the gate insulation film is formed so as to line the inner surface of the trench and a final gate electrode having the final gate length is buried therein. According to the method of manufacture, a gate structure is achieved which avoids gate offset as clearly shown in Figure 15, for example.

Turning to the rejection of Claims 1-13 under 35 U.S.C. § 103 relying upon an alleged admission of prior art, it is noted that no such admission appears in the drawings or specification as filed. In this regard, merely indicating what is conventional in Japan and known to Japanese applicants does not qualify as prior art under any section of Title 35 of the U.S. Code. Furthermore, the case law requires that an <u>actual</u> admission of "prior art" status must be made to establish such status. Accordingly, the rejection of Claims 1-13 based upon what has merely been indicated in the specification as being conventional in Japan taken with the <u>Yu</u> disclosure is traversed as being an improper rejection.

Moreover, the rejection is further traversed because even if the subject matter said to be conventional is modified by the teachings of <u>Yu</u>, the subject matter of Claims 1-13 would not be the result of such a combination.

In this regard, <u>Yu</u> teaches a method for manufacturing ultra-shallow MOSFET source and drain extensions by first forming a buried type dummy gate electrode as shown in Fig. 3. This dummy gate electrode is removed, as shown in Fig. 4, to thereby form a trench. While this much of the disclosure of <u>Yu</u> is similar to that of the present invention, <u>Yu</u> does not teach that the gate length of the dummy gate electrode should correspond to the final gate electrode length.

Moreover, as shown in Fig. 5 of <u>Yu</u>, while the upper surface of the semiconductor substrate is cut slightly at the same time the width of the trench is increased to thereby form ultra-shallow source and drain electrodes 23 and 25, the amount by which the width of the trench is increased is determined in accordance with the requisite dimension of the extension. In other words, the increase in trench width has nothing to do with and is not determined in accordance with the thickness of the final gate insulating film, unlike the present invention.

Furthermore, in Yu, gate electrode 36 is buried into a trench with a separator 32 and a gate insulating film 33 imposed between the gate electrode 36 and the trench. Also, Yu does not refer to the gate length but discloses that the width of a first formed spacer, that is, spacer 42, falls within the range of 30-80 nm (col. 4, line 18), and that of a final spacer, that is, spacer 18, falls within the range of 8-10 nm (col. 5, lines 3-4). Accordingly, if the width of the trench is increased by an amount approximately equivalent to the width of the spacer 42, the final gate length is going to be greater than the gate length of the dummy gate by about 22-70 nm. That is, Yu does not teach the method of the present invention which sets the gate length of the dummy gate electrode at the predetermined length which is the final gate length.

Accordingly, as no further issues are believed to remain outstanding in the present application, it is believed that this application is clearly in condition for formal allowance. Therefore, an early and favorable action to that effect is earnestly and respectfully requested.

Respectfully submitted,

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Marked-Up Copy
Serial No: 09/816,393
Amendment Filed:
11-29-02

IN THE TITLE

Please change the title as shown in the attached marked-up copy to read as follows:

IMPROVED METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH A BURIED GATE ELECTRODE STRUCTURE [SEMICONDUCTOR DEVICE AND A METHOD FOR MANUFACTURING THE SAME]

IN THE SPECIFICATION

Please change the paragraph beginning at page 4, line 1, as shown in the attached marked-up copy to read as follows:

In recent years, due to the microminiaturization of such elements, the gate length of the MISFET has been made very fine and the gate insulating film has been made very thin. For example, in the adoption of a silicon oxide film thinner than 2 nm (physical film thickness) as a gate insulating film, difficulty is encountered due to its tunnel current, [etc.] for example, as well as the reliability problem involved. For this reason, in place of such silicon oxide film, the adoption of a high dielectric-constant film, such as a silicon nitride film and Ta_2O_5 film, has been studied because it can be increased in thickness.

Please change the paragraph beginning at page 4, line 23, and ending on page 5, line 7, as shown in the attached marked-up copy to read as follows:

In an example of FIG. 7, after the dummy gate electrode 115 has been removed as shown in FIG. 5 to provide a trench for a final buried type gate electrode formation, a high dielectric-constant film, such as the Ta_2O_5, is formed, as a gate insulating film 201, by using the chemical vapor deposition method, [etc.] <u>for example</u>, in place of forming the above-mentioned silicon oxide film by the thermal oxidation method. The above-mentioned high dielectric-constant film, being formed by the chemical vapor deposition method and sputtering method, is formed, as shown in FIG. 7, also on the sidewall of the trench for the gate electrode formation.

Please change the paragraph beginning at page 11, line 20, and ending at page 12, line 4 as shown in the attached marked-up copy to read as follows:

After forming an isolation region 302 on a p type semiconductor substrate 301, as shown in FIG. 9, an about 5 nm-thick SiO_2 film 303 serving as a dummy gate insulating film in deposited by a thermal oxidation method on a surface of the substrate 301. Thereafter, an about 100 nm-thick polycrystalline silicon film 304 serving as a dummy gate electrode is deposited by a chemical vapor deposition method, [etc.] <u>for example</u>, on the SiO_2 film 303. Thereafter, an about 50 nm-thick silicon nitride film 305 is stacked by the chemical vapor deposition method, [etc.] <u>for example</u>, on the polycrystalline silicon film 304.

Please change the paragraph beginning at page 14, line 9, and ending at page 15, line 3, as shown in the attached marked-up copy to read as follows:

Thereafter, as shown in FIG. 14, the width of the trench 312 is enlarged by an extent corresponding to the film thickness of a desired gate insulating film. In the case of using a Ta_2O_5 film of 40 nm as the gate insulating film, an etching process is done on the sidewall surface of the trench 312 to an extent corresponding to 40 nm or more. By doing so, the trench 312 is enlarged to a trench 312' for burying a material for a final gate electrode. It is

desirable to perform an etching at this time such that both the dummy gate insulating film 303 present on the bottom and sidewall insulating film 308 present on the sidewall area of the burying trench are simultaneously etched, with an adequate selectivity to the semiconductor substrate 101. In the present embodiment using an SiO_2 for both the dummy gate insulating film 303 and sidewall insulating film 308 and a silicon for the semiconductor substrate 101, it is effective to perform an etching using a dilute HF or dilute NH_4F, [etc.] <u>for example</u>, or an isotropic dry etching using a CDE, [etc.] <u>for example</u>, that is, an etching having a selectivity to the substrate.

Please amend the paragraph beginning at page 16, line 2, as shown in the attached marked-up copy to read as follows:

Then, a 300 nm-thick tungsten, [etc.] <u>for example</u>, serving as a final gate electrode 314 is deposited by the chemical vapor deposition method, sputtering method, [etc.] <u>for example</u>, over the gate insulating film 313 on the structure shown in FIG. 15. Thereafter, a CMP polishing is done and the burying of tungsten as the gate electrode 314 in the trench 312' is completed (FIG. 16).

<u>IN THE CLAIMS</u>

Please amend the claims as follows:

--1. (Amended) A method for manufacturing a semiconductor device comprising [the steps of]:

forming a dummy gate electrode on a semiconductor substrate <u>having a predetermined length coincident with a length of a gate electrode to be formed;</u>

with the dummy gate electrode used as a mask, forming one pair of first impurity diffusion layers in [those] regions of the semiconductor substrate which are opposite to each other [through] on opposite sides of the dummy gate electrode;

forming an insulating film on the semiconductor substrate [in a way] so as to burry the dummy gate electrode[, while] and exposing an upper surface of the dummy gate electrode;

removing the dummy gate electrode [and forming] to form a first trench in the insulating film having a width corresponding to at least the predetermined length of the dummy gate electrode;

enlarging the width of the first trench on each side of the first trench by a predetermined amount [and forming] to form a second trench in the insulating film [which is greater in width than the width of the first trench], said predetermined amount being equal to or greater than a thickness of a gate insulation film to be lined on an inner surface of the second trench;

[forming a] lining the gate insulating film of said thickness along [an] the inner surface of the second trench; and

forming [a] the gate electrode in the second trench with only the gate insulating film intervening therebetween.

2. (Amended) The method according to claim 1, further comprising [the steps of]:

after forming the first impurity diffusion layers, forming a side wall insulating film on a side wall surface of the dummy gate electrode; and

with the dummy gate electrode and the sidewall insulating film used as a mask, forming second impurity diffusion layers having a deeper junction in the semiconductor substrate than the first impurity diffusion layers.

3. (Amended) The method according to claim 1, wherein the [step of] forming of a second trench includes [a step of] performing an isotropic etching on the insulating film having the first trench formed therein.

4. (Canceled).

5. (Amended) The method according to claim 1, wherein the [step of] forming of the gate insulating film includes [a step of] using an insulating material having a relative dielectric constant of above 5.

6. (Amended) The method according to claim 1, wherein the [step of] forming of a gate insulating film includes [a step of] using [one] an insulating material selected from the group consisting of Ta_2O_5, silicon nitride, Al_2O_3, $BaSrTiO_3$, Zr oxide, Hf oxide, Sc oxide, Y oxide and Ti oxide.

7. (Amended) A method of manufacturing a semiconductor device, comprising [the steps of]:

forming a first insulating film on a semiconductor substrate;

sequentially forming a first semiconductor film and a second insulating film on the first insulating film;

forming a resist pattern on the second insulating film;

with the resist pattern used as a mask, patterning the first semiconductor film and the second insulating film by an anisotropic etching to provide a stacked layer structure of the first semiconductor film and the second insulating film on the semiconductor substrate having a predetermined width coincident with a length of a gate electrode to be formed;

with the stacked layer structure used as a mask, ion-implanting an impurity in the semiconductor substrate to provide first impurity diffusion layers for a source and a drain;

forming a third insulating film over the semiconductor structure to bury the stacked layer structure;

etching back the third [insulting] insulating film to expose an upper surface of the stacked layer structure;

with the third insulating film used as a mask, removing the stacked layer structure to form a trench in the third insulating film;

after forming the trench, enlarging the width of the trench by an isotropic etching by a predetermined width amount on each side of the trench that is equal to or larger than a thickness of a fourth insulating film along an inner surface of the trench;

after enlarging the width of the trench, depositing [a] the fourth [insulting] insulating film of said thickness along [an] the inner surface of the trench; and

forming a conductive layer [of a gate electrode] on and in contact with the fourth insulating film to form said gate electrode of a length coincident with the predetermined width.

8. (Amended) The method according to claim 7, further comprising [the steps of]:

after providing the first impurity diffusion layers, forming a sidewall insulating film on a sidewall of the stacked layer structure; and

with the sidewall insulating film and the staked layer structure used as a mask, forming second impurity diffusion layers having a deeper junction in the semiconductor substrate than the first impurity diffusion layers.

9. (Amended) The method according to claim 7, wherein the [step of] enlarging of the width of the trench includes [a step of] using, as the isotropic etching, an etching treatment including HF or NH_4F.

10. (Amended) The method according to claim 7, wherein the [step of] depositing <u>of</u> [a] <u>the</u> fourth insulating film includes [a step of] depositing [a fourth insulating film] by a chemical vapor deposition method or a sputtering method.

11. (Canceled).

12. (Amended) The method according to claim 7, wherein the [step of] depositing of [a] <u>the</u> fourth insulating film includes [a step of] using an insulating material having a dielectric constant of above 5.

13. (Amended) The method according to claim 7, wherein the [step of] depositing <u>of</u> [a] <u>the</u> fourth insulating film includes [a step of] using [one] <u>an insulating material</u> selected from the group consisting of Ta_2O_5, silicon nitride, Al_2O_3, $BaSrTiO_3$, Zr oxide, Hf oxide, Sc oxide, Y oxide and Ti oxide.--